Amendments to the Drawings:

Please replace Figures 1-5 with the Replacement Sheets enclosed as Exhibit 1. Replacement Sheet of Figure 1 is a clean copy of Figure 1. Replacement Sheets for Figures 2-5 are clean copies with computer generated reference numerals (i.e., not hand written).

REMARKS

This is in response to the Office Action dated March 15, 2005.

I. SUMMARY OF OFFICE ACTION

In the Office Action, the Examiner indicated that the Applicant provisionally elected species IV without traverse. Also, the Examiner indicated Applicant designated that Claims 5-8 read on species IV, and the Examiner agreed with this statement.

Claims 5-8 were rejected under 35 USC § 103(a) as being unpatentable over Shih (U.S. Pat. No. 6,492,874) based on a view that it would have been obvious to one of ordinary skill in the art to have integrated the circuit disclosed in Shih on a wafer. The reason is that it is well known to those of ordinary skill in the art to integrate a semiconductor device in order to form a small sized integrated circuit.

The Examiner also indicated that the prior art made of record and not relied upon is considered pertinent to the Applicant's disclosure.

II. APPLICANT'S RESPONSE

A. ELECTION

Applicant acknowledges the provisional election of species IV without traverse.

B. DRAWINGS

Applicant submits concurrently herewith Replacement Sheets for Figures 1-5, as Exhibit 1. The Replacement Sheet for Figure 1 is a clean copy of Figure 1. The Replacement Sheets for Figures 2-5 are clean copies with computer generated reference numerals (i.e., not hand written). Applicant respectfully requests that the drawings be replaced with the Replacement Sheets shown in Exhibit 1.

C. CLAIMS 5-8

In the Office Action, the Examiner rejected Claim 5 under 35 USC 103(a) as being unpatentable over Shih based on a view that it would have been obvious to form an active bias circuit on the wafer the electrical circuit is formed on for the purpose of biasing the electrical circuit. Applicant respectfully disagrees.

The Shih reference involves an active bias circuit with a temperature compensation circuit such that a DC quiescent current to the amplifier is maintained at a generally fixed

value over a wide temperature range. However, there is no motivation to form the active bias circuit of Shih on the wafer the electrical circuit is formed on based on a view that the actual DC current applied to the electrical circuit will be different than the designed DC current the designers of the active bias circuit intended to apply to the electrical circuit when the Shih active bias circuit is formed on the wafer due to wafer lot variations.

The disclosure of Shih repeatedly states that a DC quiescent current is maintained at a fixed value over a wide temperature range. (col. 2, lns. 32-34; col. 2, lns. 47-48; col. 3, lns. 59-61; col. 4, lns. 29-32). As understood, the DC current actually applied by the active bias circuit is equal to the DC current which the designers of the active bias circuit intended to apply to the electrical circuit. The Shih active bias circuit produces an actual DC current that is equal to the designed DC current which the designers of the Shih active bias circuit intended to apply to the electrical circuit. However, the actual DC current produced by the Shih active bias circuit when formed on the wafer the electrical circuit is formed on is different from the designed DC current because of wafer lot variations.

As stated in the background of the invention section of the above-identified patent application, wafer lot to wafer lot variations change the required biasing voltage applied to the amplifier to operate the amplifier at its quiescent point. (Present Invention, par. 4). The wafer lot variations also change the characteristics of the active circuit bias. (Present Invention, par. 9). If the Shih active bias circuit were formed on the wafer the electrical circuit was formed on, then the Shih active bias circuit would produce an actual DC current which is not equal to the designed DC current because the component characteristics of the Shih active bias circuit would be altered due to the wafer lot variations. Hence, forming the Shih active bias circuit on the wafer the electrical circuit was formed on would render the electrical circuit inoperable because the incorrect DC current would be applied to the electrical circuit. Accordingly, there is no motivation to form the Shih active bias circuit on the wafer the electrical circuit is formed on and Claim 5 is in condition for allowance.

The dependent claims of Claim 5, namely, Claims 6-8, are also in condition for allowance for being dependent upon an allowable base Claim 5 and for containing additional patentable subject matter.

D. RELIANCE ON "WELL KNOWN" PRIOR ART

In the Office Action, as understood, the Examiner took Official Notice that "it is well known to those of ordinary skill in the art to integrate a semiconductor device in order to form a small sized integrated circuit." (Office Action, p. 3). In response, Applicant respectfully directs the Examiner's attention to MPEP § 2144.03(A) which recites that "[it] is never appropriate to rely solely on "common knowledge" in the art without evidentiary support in the record, as the principal evidence upon which a rejection was based." *In re Zurko*, 258 F.3d 1379, 1385, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001) (emphasis added). The Zurko Court also clarified that the expertise of the Board as an administrative tribunal "may provide sufficient support for conclusions [only] as to peripheral issues." Id. at 1385-86, 59 USPQ2d at 1697 (emphasis added). The purported "well known" prior art (i.e., integration of a semiconductor device to form a small sized integrated circuit" is the principal evidence upon which the Examiner's rejection is based. Without such evidence, the obviousness rejection made by the Examiner cannot be made. Accordingly, the "well known" prior art is not related to peripheral issues but is the principal evidence upon which the Examiner relies. Hence, it is not appropriate for the Examiner to rely on such evidence without evidentiary support.

MPEP § 2144.03 (C) recites that for the Applicant to adequately traverse an officially noticed fact, the "applicant must specifically point out the supposed errors in the Examiner's action, which would include stating why the noticed fact is not considered to be common knowledge or well-known in the art." MPEP § 2144.03(C) also recites that "[i]f the applicant adequately traverses the examiner's assertion of official notice, the examiner must provide documentary evidence in the next Office action if the rejection is to be maintained."

Applicant respectfully traverses the purported "well known" prior art of integration that a semiconductor device to form a small sized integrated circuit is "well known." The reason is that integration of various components may not produce a small sized integrated circuit because integration of various components may require additional components for the integrated components to function properly.

For example, the Examiner stated that it is obvious to integrate the electrical circuit and the Shih active bias circuit. However, even when the Shih active bias circuit is

integrated with the electrical circuit, the integrated electrical circuit and Shih active bias circuit is larger than if these two circuits were not integrated because an additional biasing circuit is still needed for the integrated electrical circuit and Shih active bias circuit to function properly.

In support thereof, as stated above, the actual DC current of the Shih active bias circuit is different than the designed DC current when the Shih active bias circuit is integrated onto the wafer the electrical circuit is formed on. As a result, the electrical circuit is not properly biased by the Shih active bias circuit when the Shih active bias circuit is integrated with the electrical circuit. As such, the electrical circuit requires a second biasing circuit in addition to the Shih active bias circuit to properly bias the electrical circuit. The properly biased electrical circuit is larger compared to the electrical circuit without the Shih active bias circuit integrated therewith because the properly biased electrical circuit requires the second biasing circuit, whereas, the electrical circuit without the Shih active bias circuit integrated therewith does not require the second biasing circuit. Hence, the purported "well known" prior art is not considered to be "well-known."

Applicant has stated why the noticed fact is not considered to be "well known" in the art. As such, Applicant has adequately traversed the finding of the purported "well known" prior art.

E. NEW CLAIMS 21-22

By this Amendment, Applicant respectfully requests entry of new Claims 21-22 into the prosecution of the above-identified patent application. The basis for new Claims 21-22 may be found within the specification as filed, namely, at paragraphs 30 and 31. Further, Applicant respectfully request entry of new paragraphs 0014.1 and 0014.2, as shown above, to provide antecedent basis for the term offset within the specification.

New Claims 21-22 are directed subject matter similar as that of Claim 5. As such, Applicant respectfully submits that Claims 21-22 are believed to be in condition for allowance for the same reasons that Claim 5 is believed to be in condition for allowance.

F. PRIOR ART

Applicant acknowledges receipt of the prior art made of record and not relied upon, but considered by the Examiner to be pertinent to Applicant's disclosure. Applicant

respectfully submits that the cited prior art, either alone or in combination, does not anticipate, suggest, or make obvious the instantly claimed invention.

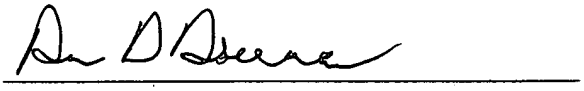
III. CONCLUSION

For the foregoing reasons, Applicant respectfully submits that all the stated grounds of rejection have been overcome, and that Claims 5-8 and 21-22 are in condition for allowance. An early notice of allowance is therefore respectfully requested.

Should the Examiner have any suggestions for expediting allowance of the application, the Examiner is invited to contact the Applicant's representative at the telephone number listed below.

If any additional fee is required, please charge Deposit Account Number 19-4330.

Respectfully submitted,

Date: May 10, 2005 By: 

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